ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device including a memory cell array region having reduced influence of disturbance noise and divided into row blocks for every sub-bitline subordinate to main bitlines. One end of each sub bitline is connected to the main bitline through a first sub bitline select switch. The other end of the sub bitline is connected to a common potential supply line through a second sub-bitline select switch which is turned on complementarily with the first sub-bitline select switch.